IN THE CLAIMS:

1. (Currently Amended) A method of forming at least one field effect transistor on a substrate, the method comprising:

forming a gate insulation layer for said at least one field effect transistor on a surface of said substrate;

after forming said gate insulation layer, forming a strained surface layer on a surface of said substrate by implanting germanium ions ~~of at least one heavy inert material~~ through said gate insulation layer and said surface of said substrate;

forming at least one gate structure above said strained surface layer; and

performing additional process steps to manufacture said at least one field effect transistor, wherein a thermal budget in manufacturing the at least one field effect transistor is adjusted to substantially avoid silicon grid restoration in the strained surface layer.

2. (Currently Amended) The method of claim 1, wherein, in forming said strained surface layer, ions of at least one of xenon~~,~~ and argon~~, germanium, silicon, or a combination thereof,~~ are also implanted.

3. (Original) The method of claim 1, wherein the implanting energy is selected in the range of approximately 10-100 keV.

4. (Original) The method of claim 1, wherein the implanting dose is selected in the range of approximately $10^{13}/cm^2 - 10^{16}/cm^2$.

5. (Canceled)

6. (Original) The method of claim 1, wherein said substrate comprises one of silicon and germanium or a combination thereof.

7. (Original) The method of claim 1, wherein said field effect transistor is one of an NMOS, a PMOS and a CMOS transistor.

8.-17. (Canceled)

18. (Currently Amended) A method of forming at least one field effect transistor on a substrate, the method comprising:

forming a gate insulation layer for said at least one field effect transistor on a surface of said substrate;

forming a strained surface layer on a surface of said substrate by implanting germanium ions ~~of at least one heavy inert material~~ through said gate insulation layer and into said substrate, said strained surface layer having a thickness less than 20 nm; ~~and~~

forming at least one gate electrode structure above said gate insulation layer after forming said strained surface layer; and

performing additional process steps to manufacture said at least one field effect transistor, wherein a thermal budget in manufacturing the field effect transistor is adjusted to substantially avoid silicon grid restoration in the strained surface layer.

19. (Currently Amended) The method of claim 18, wherein, in forming said strained surface layer, ions of at least one of xenon, and argon~~, germanium, silicon, or a combination thereof,~~ are also implanted.

20. (Canceled)

21. (Canceled)

22. (New) A method of forming at least one field effect transistor on a substrate, the method comprising:

forming a gate insulation layer for said at least one field effect transistor on a surface of said substrate;

after forming said gate insulation layer, forming a strained surface layer on a surface of said substrate by implanting xenon ions through said gate insulation layer and said surface of said substrate;

forming at least one gate structure above said strained surface layer; and

performing additional process steps to manufacture said at least one field effect transistor, wherein a thermal budget in manufacturing the at least one field effect transistor is adjusted to substantially avoid silicon grid restoration in the strained surface layer.

23. (New) The method of claim 22, wherein, in forming said strained surface layer, ions of at least one of argon and germanium ions are also implanted.

24. (New) A method of forming at least one field effect transistor on a substrate, the method comprising:

forming a gate insulation layer for said at least one field effect transistor on a surface of said substrate;

forming a strained surface layer on a surface of said substrate by implanting xenon ions through said gate insulation layer and into said substrate, said strained surface layer having a thickness less than 20 nm;

forming at least one gate electrode structure above said gate insulation layer after forming said strained surface layer; and

performing additional process steps to manufacture said at least one field effect transistor, wherein a thermal budget in manufacturing the field effect transistor is adjusted to substantially avoid silicon grid restoration in the strained surface layer.

25. (New) The method of claim 24, wherein, in forming said strained surface layer, ions of at least one of argon and germanium ions are also implanted.

26. (New) A method of forming at least one field effect transistor on a substrate, the method comprising:

forming a gate insulation layer for said at least one field effect transistor on a surface of said substrate;

after forming said gate insulation layer, forming a strained surface layer on a surface of said substrate by implanting argon ions through said gate insulation layer and said surface of said substrate;

forming at least one gate structure above said strained surface layer; and

performing additional process steps to manufacture said at least one field effect transistor, wherein a thermal budget in manufacturing the at least one field effect transistor is adjusted to substantially avoid silicon grid restoration in the strained surface layer.

27. (New) The method of claim 26, wherein, in forming said strained surface layer, ions of at least one of xenon and germanium are also implanted.

28. (New) A method of forming at least one field effect transistor on a substrate, the method comprising:

forming a gate insulation layer for said at least one field effect transistor on a surface of said substrate;

forming a strained surface layer on a surface of said substrate by implanting argon ions through said gate insulation layer and into said substrate, said strained surface layer having a thickness less than 20 nm;

forming at least one gate electrode structure above said gate insulation layer after forming said strained surface layer; and

performing additional process steps to manufacture said at least one field effect transistor, wherein a thermal budget in manufacturing the field effect transistor is adjusted to substantially avoid silicon grid restoration in the strained surface layer.

29. (New) The method of claim 28, wherein, in forming said strained surface layer, ions of at least one of xenon and germanium are also implanted.